

Notice of References Cited

Application/Control No.

09/893,023

Applicant(s)/Patent Under
Reexamination
O'MAHONY ET AL.

Examiner

A. Sefer

Art Unit

2826

Page 1 of 1

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	U	Restle et al. "Desgning the Best Clock Distribution Network" IEEE Symposium on VLSI Circuits Digest of Techincal Papers, 1998.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign